

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-5. (Canceled).

6. (Currently amended) A method for manufacturing a silicon wafer ~~which manufactures said silicon wafer according to claim 1~~, comprising:

removing an oxide film on a surface of a silicon wafer;

after removing, vacancy heat treating for forming new vacancies in an interior of said silicon wafer by means of a heat treatment of said silicon wafer at a temperature of 1135 to 1170°C in an atmosphere of gas containing nitrogen containing NH₃ for a period of between one second and 60 seconds so as to nitride the surface of said silicon wafer;

quenching said silicon wafer after said vacancy heat treating; and

SF nuclei heat treating for agglomerates interstitial silicon released during precipitation of oxygen from vacancies injected by said vacancy treating, to form stacking fault nuclei, thereby forming an SF nuclei layer of high stacking fault nuclei density in the interior near the surface,

wherein during said vacancy heat treating, purging is conducted to remove oxygen from said atmosphere surrounding said silicon wafer, and in said SF nuclei heat treating, a rate of temperature increase is set to 10°C/minute or less, a heat treatment temperature is set to 1100°C or higher, and said heat treatment temperature is maintained for one hour or more.

7.-18. (Canceled).

19. (Currently amended) A method for manufacturing a silicon wafer ~~comprising heat treating said silicon wafer manufactured by the method of~~ according to claim 6, further comprising heat treating said silicon wafer to form at least a defect-free layer on a ~~in the~~ surface of said silicon wafer.

20. (Currently amended) A silicon wafer manufactured by said method of claim 19 and comprises:

a DZ layer in the surface thereof; and

an SF nuclei layer of high stacking fault nuclei density in the interior near the surface, wherein stacking fault nuclei which are formed from agglomeration of interstitial silicon are distributed throughout an entire in-plane direction of said SF nuclei layer, and a density of said stacking fault nuclei is set in a range of between $0.5 \times 10^8 \text{ cm}^{-3}$ and $1 \times 10^{11} \text{ cm}^{-3}$.

21.-24. (Canceled).

25. (Currently amended) A method for manufacturing a silicon wafer according to claim 6, wherein the method further comprises pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing said ingot to manufacture said silicon wafer, and

wherein said ingot is pulled such that a ratio V/G of, a rate V at which said ingot is pulled, and a temperature gradient G of said ingot in a vertical direction in a vicinity of an interface between said silicon melt in said crucible and said ingot, is between $0.20 \text{ mm}^2/\text{C}\cdot\text{minute}$ and $0.25 \text{ mm}^2/\text{C}\cdot\text{minute}$.

26. (Currently amended) A method for manufacturing a silicon wafer according to claim 6, wherein the method further comprises pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing said ingot to manufacture a silicon wafer, and

wherein nitrogen is added while pulling said ingot, to set an internal nitrogen concentration within a range of between $5 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{15} \text{ cm}^{-3}$.

27. (Previously presented) A method for manufacturing a silicon wafer according to claim 6, wherein in said SF nuclei heat treating, while interstitial silicon is injected in a surface of said silicon wafer, said stacking fault nuclei are formed.

28. (Previously presented) A method for manufacturing a silicon wafer according to claim 6, wherein in said SF nuclei heat treating, said stacking fault nuclei are formed from only said interstitial silicon released during precipitation of oxygen.

29. (New) A method for manufacturing a silicon wafer according to claim 6, wherein said silicon wafer is subjected to said SF nuclei heat treating in a state in which a high concentration of vacancies are formed in the interior near the surface.

30. (New) A silicon wafer, which is manufactured by the method for manufacturing a silicon wafer of claim 6, and comprises an SF nuclei layer of high stacking fault nuclei density in the interior near the surface, wherein stacking fault nuclei which are formed from agglomeration of interstitial silicon are distributed throughout an entire in-plane direction of said silicon wafer, and a density of said stacking fault nuclei is set in a range of between $0.5 \times 10^8 \text{ cm}^{-3}$ and $1 \times 10^{11} \text{ cm}^{-3}$.

31. (New) A silicon wafer according to claim 30, which is cut from an ingot formed from a perfect region in which interstitial silicon-type point defect agglomerates and vacancy-type point defect agglomerates are substantially non-existent.

32. (New) A silicon wafer according to claim 30, which is cut from an ingot formed from a region in which vacancy-type point defects are dominant.